AMENDMENTS TO THE CLAIMS

Please amend claims 1-3, 5-7, 16-17, 19-21, 26, 29, and 31-35, as follows. A complete listing of pending claims is provided below.

1. (Currently Amended) A method for ~~generating a test vector~~ performing assertion checking for functional verification of circuits comprising:

providing a representation of a circuit, the representation comprising a control logic component and a datapath logic component;

reading one or more vector generation targets;

performing word-level ATPG justification on the control logic component to obtain a control logic solution;

extracting one or more arithmetic functions for the datapath logic component based on the control logic solution; and

solving the one or more arithmetic functions using a modular constraint solver, the modular constraint solver being based on a modular number system.

2. (Currently Amended) The method of Claim 1, wherein the word-level ATPG justification comprises performing word-level implication on circuit components related to the one or more vector generation targets.

3. (Currently Amended) The method of Claim 1, wherein solving the one or more arithmetic functions comprises:

determining possible solutions for ~~the~~ one or more nonlinear equations; and

solving ~~the~~ one or more linear equations using one possible solution for the one or more nonlinear equations as boundary conditions.

4. (Original) The method of Claim 1 further comprising:

dependent on the outcome of solving the one or more arithmetic functions, backtracking to perform word-level ATPG justification on the control logic component to obtain a second control logic solution;

extracting one or more arithmetic functions for the datapath logic component based on the second control logic solution; and

solving the one or more arithmetic functions using the modular constraint solver.

5. (Currently Amended) The method of Claim 1, wherein ~~the~~ at least one vector generation target comprises a signal value.

6. (Currently Amended) The method of Claim 1, wherein ~~the~~ at least one vector generation target comprises a relation among a set of signals.

7. (Currently Amended) The method of Claim 1, wherein ~~the~~ at least one vector generation target comprises a sequence of relations among a set of signals.

8.-14. (Canceled)

15. (Original) A computer-readable storage medium having stored thereon computer instructions that, when executed by a computer, cause the computer to:

provide a representation of a circuit, the representation comprising a control logic component and a datapath logic component;

read one or more vector generation targets;

perform word-level ATPG justification on the control logic component to obtain a control logic solution;

extract one or more arithmetic functions for the datapath logic component based on the control logic solution; and

solve the one or more arithmetic functions using a modular constraint solver, the modular constraint solver being based on a modular number system.

16. (Currently Amended) The computer-readable storage medium of Claim 15, wherein the computer instructions that perform word-level ATPG justification further comprise computer instructions that, when executed by a computer, cause the computer to perform word-level implication on circuit components related to the one or more vector generation targets.

17. (Currently Amended) The computer-readable storage medium of Claim 15, wherein the computer instructions that solve the one or more arithmetic functions further comprise computer instructions that, when executed by a computer, cause the computer to:

determine possible solutions for ~~the~~ one or more nonlinear equations; and

solve ~~the~~ one or more linear equations using one possible solution for the one or more nonlinear equations as boundary conditions.

18. (Original) The computer-readable storage medium of Claim 15, wherein the computer instructions that solve the one or more arithmetic functions further comprise computer instructions that, when executed by a computer, cause the computer to:

dependent on the outcome of solving the one or more arithmetic functions, backtrack to perform word-level ATPG justification on the control logic component to obtain a second control logic solution;

extract one or more arithmetic functions for the datapath logic component based on the second control logic solution; and

solve the one or more arithmetic functions using the modular constraint solver.

19. (Currently Amended) The computer-readable storage medium of Claim 15, wherein ~~the~~ at least one vector generation target comprises a signal value.

20. (Currently Amended) The computer-readable storage medium of Claim 15, wherein ~~the~~ at least one vector generation target comprises a relation among a set of signals.

21. (Currently Amended) The computer-readable storage medium of Claim 15, wherein ~~the~~ at least one vector generation target comprises a sequence of relations among a set of signals.

22.-25. (Canceled)

26. (Currently Amended) The computer-readable storage medium of Claim 15, wherein the word-level ATPG justification is performed by performing a word-level implication, the word-level implication ~~comprises~~ comprising a decision on at least one control signal.

27. (Previously Presented) The computer-readable storage medium of Claim 26, wherein the word-level implication is performed on the at least one control signal.

28. (Previously Presented) The computer-readable storage medium of Claim 15, further comprising computer instructions that, when executed by a computer, cause the computer to:

extract one or more arithmetic functions based on the ATPG justification; and

solve the one or more arithmetic functions using the modular constraint solver.

29. (Currently Amended) A system for ~~generating a test vector~~ performing assertion checking for functional verification of circuits comprising:

means for providing a representation of a circuit, the representation comprising a control logic component and a datapath logic component;

means for reading one or more vector generation targets;

means for performing word-level ATPG justification on the control logic component to obtain a control logic solution;

means for extracting one or more arithmetic functions for the datapath logic component based on the control logic solution; and

means for solving the one or more arithmetic functions using a modular constraint solver, the modular constraint solver being based on a modular number system.

30. (Previously Presented) The system of Claim 29, wherein the means for performing the word-level ATPG justification comprises means for performing word-level implication on circuit components related to the one or more targets.

31. (Currently Amended) The system of Claim 29, wherein the means for solving the one or more arithmetic functions comprises:

means for determining possible solutions for ~~the~~ one or more nonlinear equations; and

means for solving ~~the~~ one or more linear equations using one possible solution for the one or more nonlinear equations as boundary conditions.

32. (Currently Amended) The system of Claim 29, further comprising:

~~means for~~ dependent on the outcome of solving the one or more arithmetic functions, means for backtracking to perform word-level ATPG justification on the control logic component to obtain a second control logic solution;

means for extracting one or more arithmetic functions for the datapath logic component based on the second control logic solution; and

means for solving the one or more arithmetic functions using the modular constraint solver.

33. (Currently Amended) The method of Claim 29, wherein ~~the~~ at least one vector generation target comprises a signal value.

34. (Currently Amended) The method of Claim 29, wherein ~~the~~ at least one vector generation target comprises a relation among a set of signals.

35. (Currently Amended) The method of Claim 29, wherein ~~the~~ at least one vector generation target comprises a sequence of relations among a set of signals.